REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device types 05 through 10 with vendor cage 88379. Redrew entire document.	96-07-03	K.A. Cottongim
B	Added case outline M. Added vendor cage 54230 for device types 05 through 10.	96-09-27	K.A. Cottongim

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B								
SHEET	15	16	17	18	20	21	22	23	24	25	26	27								

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
95-11-13

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, MEMORY, DIGITAL, 512K x 32-BIT, STATIC RANDOM ACCESS MEMORY, CMOS

SIZE	CAGE CODE	
A	**67268**	**5962-94611**

SHEET 1 OF 27

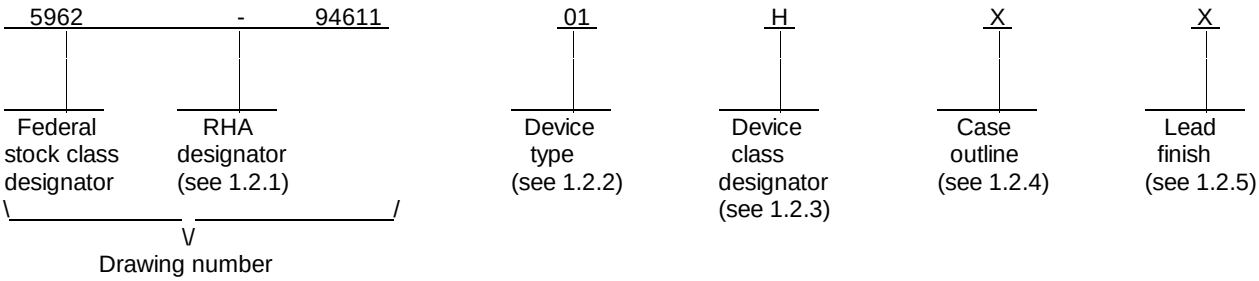
DESC FORM 193
JUL 94

5962-E557-96

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). This drawing describes device requirements for hybrid microcircuits to be processed in accordance with MIL-PRF-38534. Two product assurance classes, military high reliability (device class H) and space application (device class K) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WS512K32-120Q	512K X 32-BIT SRAM	120 ns
02	WS512K32-100Q	512K X 32-BIT SRAM	100 ns
03	WS512K32-85Q	512K X 32-BIT SRAM	85 ns
04	WS512K32-70Q	512K X 32-BIT SRAM	70 ns
05	ACT-S512K32N-055Q,WS512K32-55Q	512K X 32-BIT SRAM	55 ns
06	ACT-S512K32N-045Q,WS512K32-45Q	512K X 32-BIT SRAM	45 ns
07	ACT-S512K32N-035Q,WS512K32-35Q	512K X 32-BIT SRAM	35 ns
08	ACT-S512K32N-025Q,WS512K32-25Q	512K X 32-BIT SRAM	25 ns
09	ACT-S512K32N-020Q,WS512K32-20Q	512K X 32-BIT SRAM	20 ns
10	ACT-S512K32N-017Q,WS512K32-17Q	512K X 32-BIT SRAM	17 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
H or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	See figure 1	68	Ceramic, quad flatpack, dual cavity
X	See figure 1	66	Hex-in-line, single cavity, with standoffs
Y	See figure 1	68	Ceramic, quad flatpack, single cavity

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534 for classes H and K. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Signal voltage range (V_g)	-0.5 V dc to V_{CC} +0.5 V dc
Power dissipation (P_D):	
Device types 01-04	2.2 W
Device types 05 and 06	3.0 W
Device types 07 and 08	3.6 W
Device types 09 and 10	4.4 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_j)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.3 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} +0.3 V dc
Output low voltage, maximum (V_{OL})	+0.4 V dc
Output high voltage, minimum (V_{OH})	+2.4 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. Unless otherwise specified, the following specification, standards, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

PERFORMANCE

MIL-PRF-8534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Microcircuit Drawings.

(Copies of the specification, standards, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38534 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figure 4 and 5.

3.2.5 Block diagram. The block diagram shall be as specified on figure 6.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in QML-38534.

3.6 Manufacturer eligibility. In addition to the general requirements of MIL-PRF-38534, the manufacturer of the part described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DSCC-VA shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38534 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ Vdc $\le V_{CC} \le +5.5$ Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC parameters							
Operating supply current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$ $V_{CC} = 5.5$ V dc 2/ f = 5 MHz	1,2,3	01,02		200	mA
		f = 5 MHz		03,04		200	
		f = 5 MHz		05-10		520	
		f = 18.2 MHz		05		550	
		f = 22.2 MHz		06		550	
		f = 28.6 MHz		07		550	
		f = 40 MHz		08		600	
		f = 50 MHz		09		650	
		f = 58.8 MHz		10		700	
Standby current	I_{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$ f = 5 MHz $V_{CC} = 5.5$ V dc 2/	1,2,3	01,02		4	mA
				03,04		4	
				05-10		80	
		f = 18.2 MHz		05		150	
		f = 22.2 MHz		06		150	
		f = 28.6 MHz		07		190	
		f = 40 MHz		08		190	
		f = 50 MHz		09		240	
		f = 58.8 MHz		10		240	
Input Leakage current	I_{LI}	$V_{CC} = 5.5$ V dc, V_{IN} = GND or V_{CC}	1,2,3	All		10	µA
Output Leakage current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$ V_{OUT} = GND or V_{CC}	1,2,3	All		10	µA
Output Low voltage	V_{OL}	$V_{CC} = +4.5$ V dc, $I_{OL} = 2.1$ mA	1,2,3	01-06		0.4	V
		$V_{CC} = +4.5$ V dc, $I_{OL} = 8$mA	1,2,3	07-10		0.4	V
Output high voltage	V_{OH}	$V_{CC} = +4.5$ V dc, $I_{OH} = -1.0$ mA	1,2,3	01-06	2.4		V
		$I_{OH} = -4.0$ mA	1,2,3	07-10	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ Vdc $\le V_{CC} \le +5.5$ Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data Retention Characteristics							
Data retention supply voltage	V_{DR}	$\overline{CS} \ge V_{CC}$ - 0.2 V dc	1,2,3	All	2.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3 V dc	1,2,3	01,02 03,04 05 06 07,08 09,10		1.6 1.6 4.0 4.0 8.0 8.0	mA
Capacitance							
$\overline{OE}$ capacitance 3/	C_{OE}	V_{IN} = 0 V dc , f = 1.0 MHz $T_A = +25°C$	4	All		50	pF
$\overline{WE}$ 1-4 capacitance 3/	C_{WE}	V_{OUT} = 0 V dc , f = 1.0 MHz $T_A = +25°C$	4	All		20	pF
$\overline{CS}$ capacitance 3/	C_{CS}	V_{IN} = 0 V dc , f = 1.0 MHz $T_A = +25°C$	1,2,3	All		20	pF
D_{0-31} capacitance 3/	$C_{I/O}$	V_{OUT} = 0 V dc , f = 1.0 MHz $T_A = +25°C$	1,2,3	All		20	pF
A_{0-16} capacitance 3/	C_{AD}	VOUT = 0 V dc , f = 1.0 MHz $T_A = +25°C$	1,2,3	All		50	pF
Functional tests							
Functional tests		See 4.3.1c	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ Vdc $\le V_{CC} \le +5.5$ Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle timing characteristics							
Read cycle time	t_{RC}	See figure 4	9,10,11	01 02 03 04 05 06 07 08 09 10	120 100 85 70 55 45 35 25 20 17		ns
Address access time	t_{AA}	See figure 4	9,10,11	01 02 03 04 05 06 07 08 09 10		120 100 85 70 55 45 35 25 20 17	ns
Output hold from Address change	t_{OH}	See figure 4	9,10,11	01-04 05-10	5 0		ns
Chip select access time	t_{ACS}	See figure 4	9,10,11	01 02 03 04 05 06 07 08 09 10		120 100 85 70 55 45 35 25 20 17	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc +4.5 Vdc $\le V_{CC} \le$ +5.5 Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle timing characteristics - Continued.							
Output Enable to Output valid	t_{OE}	See figure 4	9,10,11	01 02 03 04 05-07 08 09 10		60 50 40 35 25 12 10 9	ns
Chip Select to output In low impedance 3/	t_{CLZ}	See figure 4	9,10,11	01,02 03,04 05-07 08,09 10	10 10 4 2 2		ns
Output Enable to output In low impedance 3/	t_{OLZ}	See figure 4	9,10,11	01,02 03,04 05-10	5 5 0		ns
Chip Select high to Output in high Impedance 3/	t_{CHZ}	See figure 4	9,10,11	01,02 03,04 05,06 07 08-10		35 25 20 15 12	ns
Output Enable high to Output in high Impedance 3/	t_{OHZ}	See figure 4	9,10,11	01,02 03,04 05,06 07 08-10		35 25 20 15 12	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ Vdc $\le V_{CC} \le +5.5$ Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle AC timing.							
Write cycle time	t_{WC}	See figure 5	9,10,11	01 02 03 04 05 06 07 08 09 10	120 100 85 70 55 45 35 25 20 17		ns
Chip Select to end of write	t_{CW}	See figure 5	9,10,11	01 02 03 04 05 06 07 08 09,10	100 80 75 60 50 35 30 20 15		ns
Address valid to end of write	t_{AW}	See figure 5	9,10,11	01 02 03 04 05 06 07 08 09,10	100 80 75 60 50 35 30 20 15		ns
Data Valid to end of Write	t_{DW}	See figure 5	9,10,11	01,02 03,04 05,06 07 08 09,10	40 30 25 20 15 12		ns
Address setup time	t_{AS}	See figure 5	9,10,11	01-04 05-10	0 2		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc +4.5 Vdc $\le V_{CC} \le$ +5.5 Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle AC timing - Continued.							
Write pulse width	t_{WP}	See figure 5	9,10,11	01,02 03,04 05 06 07 08 09,10	60 50 40 35 25 17 15		ns
Write enable to output in high impedance 3/	t_{WHZ}	See figure 5	9,10,11	01,02 03,04 05,06 07 08 09 10		35 25 20 15 13 11 9	ns
Address hold time	t_{AH}	See figure 5	9,10,11	01-06 07,08 09 10	5 2 1 0		ns
Output active from end of write 3/	t_{OW}	See figure 5	9,10,11	01,02 03,04 05-10	5 5 0		ns
Data hold time	t_{DH}	See figure 5	9,10,11	All	0		ns

1/ Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V
Input rise and fall times: 5 nanoseconds
Input and output timing reference level: 1.5 V $\pm$ 0.5 V
Output loading: See Figure 7

Unless otherwise specified, the DC test conditions are as follows:
V_{IL} = 0.3 V and $V_{IH} = V_{CC}$ - 0.3 V

2/ $f = 1 / t_{AA}$.

3/ Parameters shall be tested as part of device characterization and after design and process change. Parameters shall be to the limits specified in Table 1 for all lots not specifically tested.

Case outline M

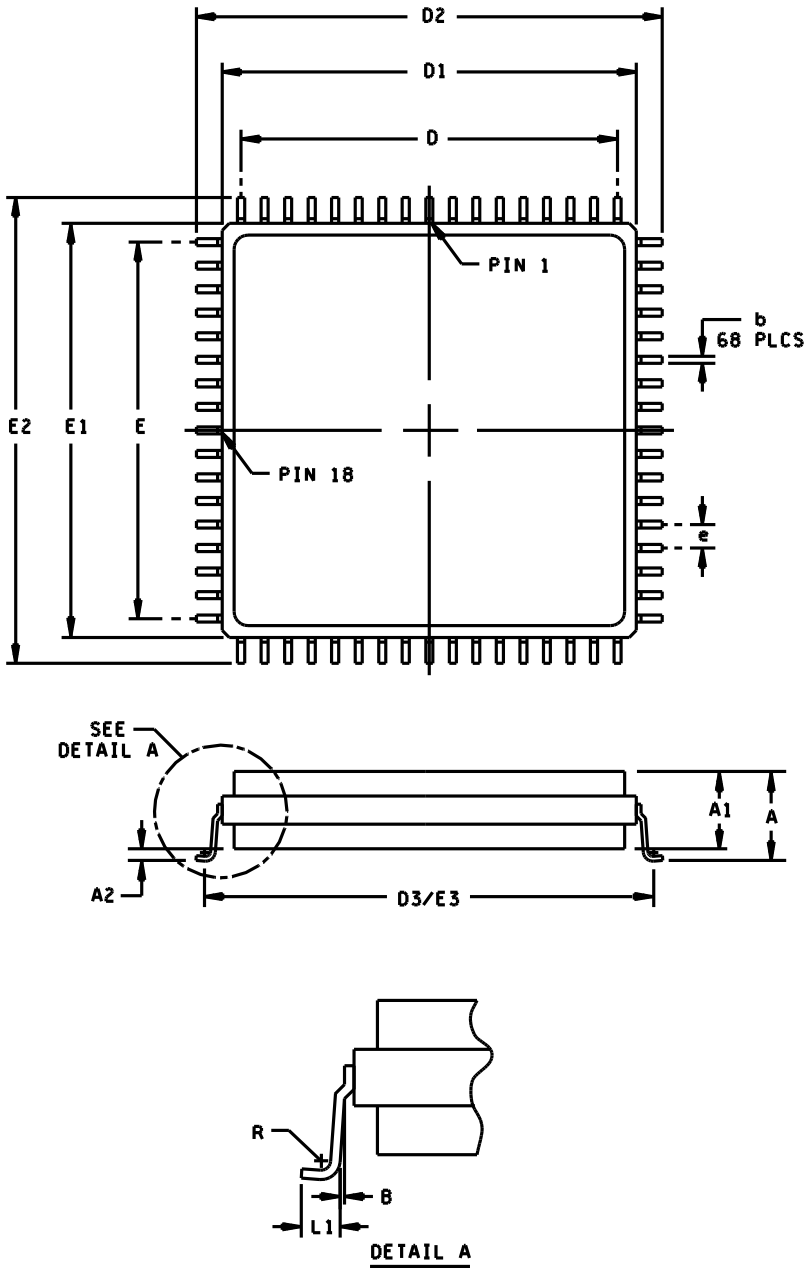


FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-94611**
		REVISION LEVEL B	SHEET **11**

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.10	0.150	0.200
A1	3.76	4.72	0.148	0.186
A2	0.00	0.38	0.000	0.020
b	0.33	0.43	0.013	0.017
D/E	20.3 BSC		0.800 BSC	
D1/E1	22.10	22.65	0.870	0.890
D2/E2	24.89	25.35	0.980	1.000
D3/E3	23.75	24.28	0.936	0.956
e	1.27 BSC		0.050 BSC	
R	0.13		0.005	
L1	0.89	1.14	0.035	0.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. Case outline M is a dual cavity package.

FIGURE 1. Case outline(s) - Continued.

Case outline X.

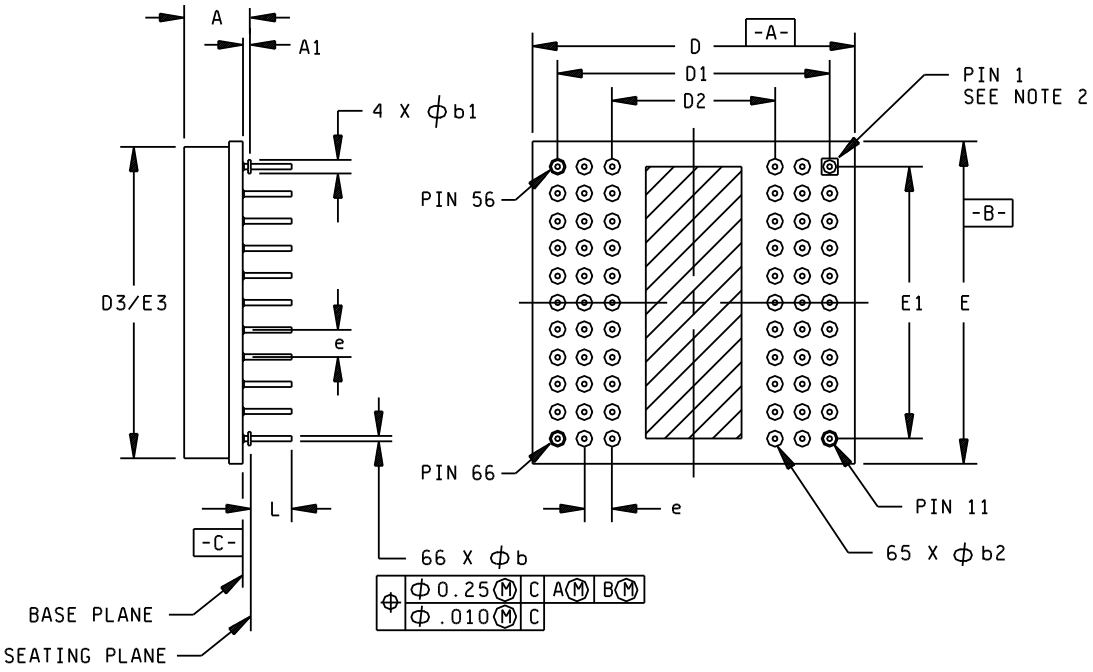


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.83	6.22	0.190	0.245
A1	0.64	0.89	0.025	0.035
⌀b	0.41	0.51	0.016	0.020
⌀b1	1.14	1.40	0.045	0.055
⌀b2	1.65	1.91	0.065	0.075
D/E	34.80	35.56	1.370	1.400
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		0.606 BSC	
D3	34.04	34.29	1.340	1.350
e	2.54 BSC		0.100 BSC	
L	3.68	3.94	0.145	0.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only. Pin 1 is identified by 0.070 " square pad.
3. For solder lead finish, dimension ϕb will increase by +0.003" (+.008 mm).

FIGURE 1. Case outline(s) - Continued.

Case outline Y.

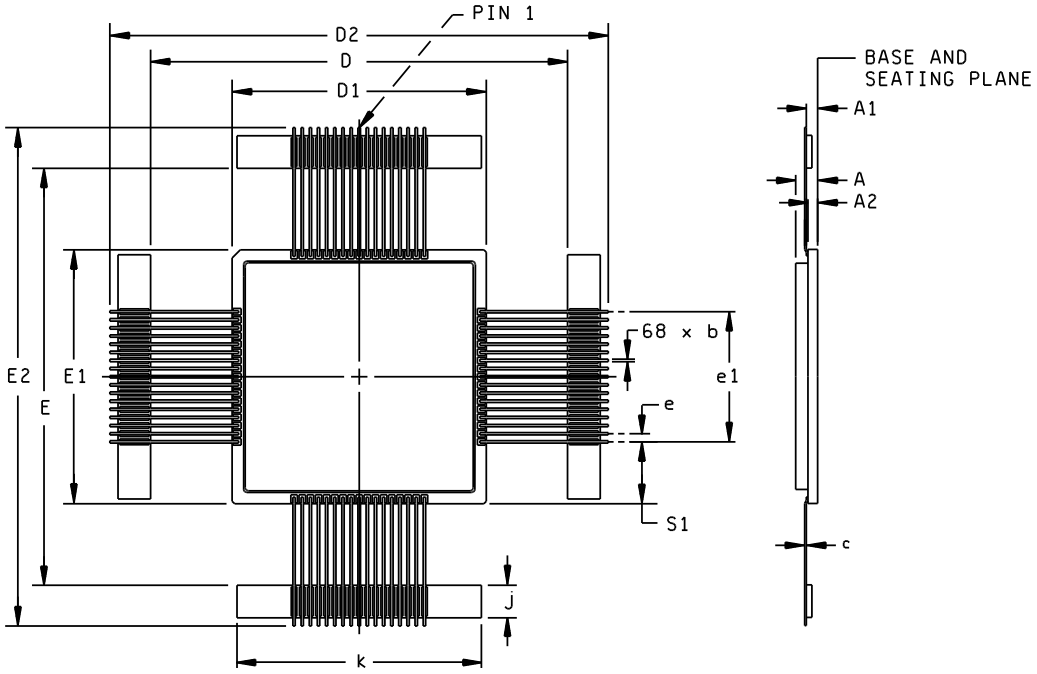


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.92	3.56	0.115	0.140
A1	1.14	1.91	0.045	0.075
A2	1.14	1.39	0.045	0.055
b	0.31	0.46	0.012	0.018
C	0.23	0.31	0.009	0.012
D/E	63.63	66.42	2.505	2.615
D1/E1	39.24	40.01	1.545	1.575
D2/E2	73.28	79.63	2.885	3.135
e	1.27 BSC		0.050 BSC	
e1	20.32 BSC		0.800 BSC	
j	4.83	5.33	0.190	0.210
k	37.72	38.48	1.485	1.515
S1	9.65 BSC		0.380 BSC	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. For solder lead finish, dimension b will increase by +0.003" (+.008 mm).

FIGURE 1. Case outline - Continued.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	M	Case outline	M	Case outline	M	Case outline	M
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS3}$	19	I/O8	36	$\overline{CS2}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	$\overline{WE2}$	55	I/O21
5	A3	22	I/O11	39	$\overline{WE3}$	56	I/O20
6	A2	23	I/O12	40	$\overline{WE4}$	57	I/O19
7	A1	24	I/O13	41	A18	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE1}$
17	I/O7	34	$\overline{CS1}$	51	I/O24	68	$\overline{CS4}$

FIGURE 2. Terminal connections.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	X	Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O8	18	A12	35	I/O25	52	$\overline{WE3}$
2	I/O9	19	V_{CC}	36	I/O26	53	$\overline{CS3}$
3	I/O10	20	$\overline{CS1}$	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/03	39	NC	56	I/O31
6	A15	23	I/015	40	A8	57	I/O30
7	A16	24	I/O14	41	A9	58	I/O29
8	A17	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	$\overline{OE}$	44	I/O18	61	A1
11	I/O2	28	A18	45	V_{CC}	62	A2
12	$\overline{WE2}$	29	$\overline{WE1}$	46	$\overline{CS4}$	63	I/O23
13	$\overline{CS2}$	30	I/O7	47	$\overline{WE4}$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

FIGURE 2. Terminal connections - Continued.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	Y	Case outline	Y	Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS1}$	19	I/O8	36	$\overline{CS4}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	A18	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE}$
17	I/O7	34	$\overline{CS2}$	51	I/O24	68	$\overline{CS3}$

FIGURE 2. Terminal connections - Continued.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	MODE
V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Read
V_{IH}	X	X	High Z	Standby
V_{IL}	V_{IH}	V_{IH}	High Z	Output disable
V_{IL}	V_{IH}	V_{IL}	D_{IN}	Write

NOTES:
1. V_{IH} = High Logic Level
2. V_{IL} = Low Logic Level
3. X = Do not care (either high or low)
4. High Z = High Impedance State

FIGURE 3. Truth table.

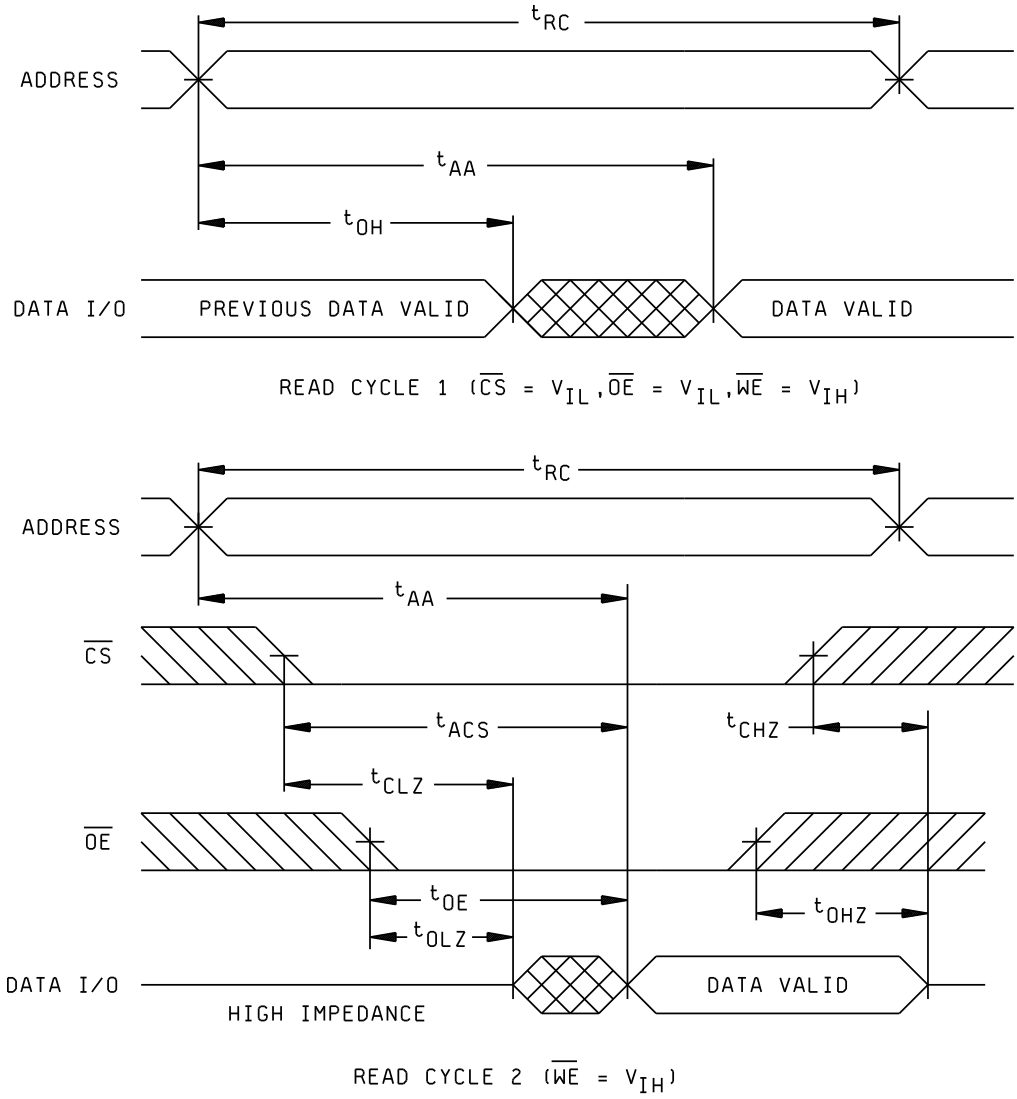
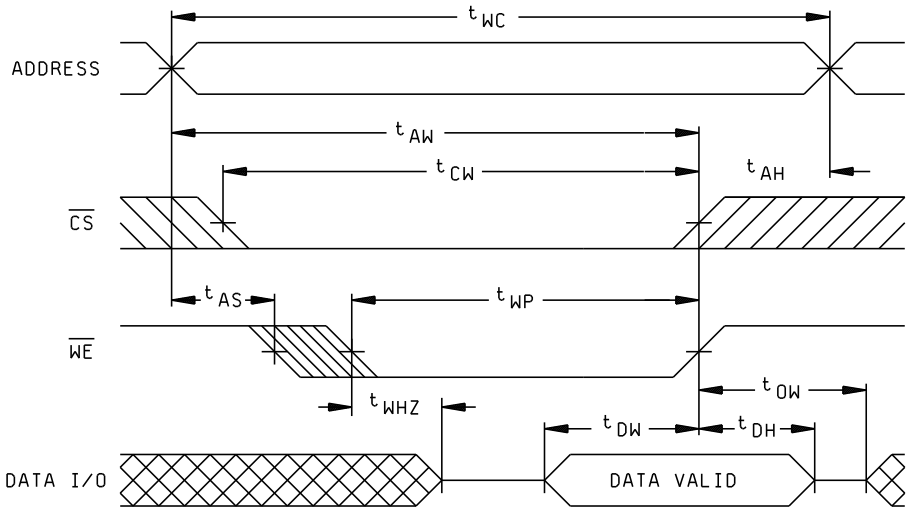
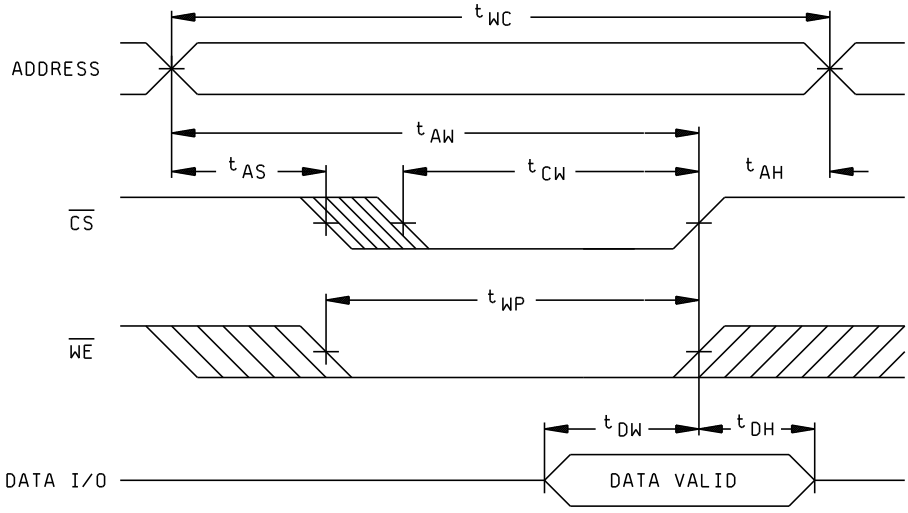


FIGURE 4. Read cycle timing diagram.



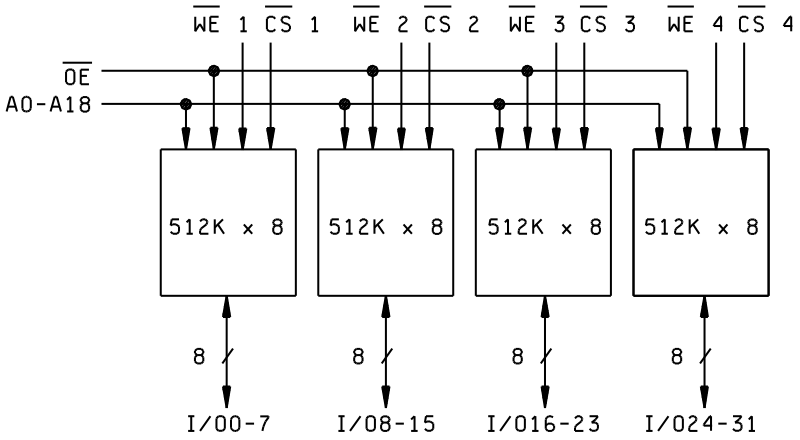
WRITE CYCLE 1 $\overline{WE}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED

FIGURE 5. Write cycle timing diagram.

Case outlines M and X



Case outline Y

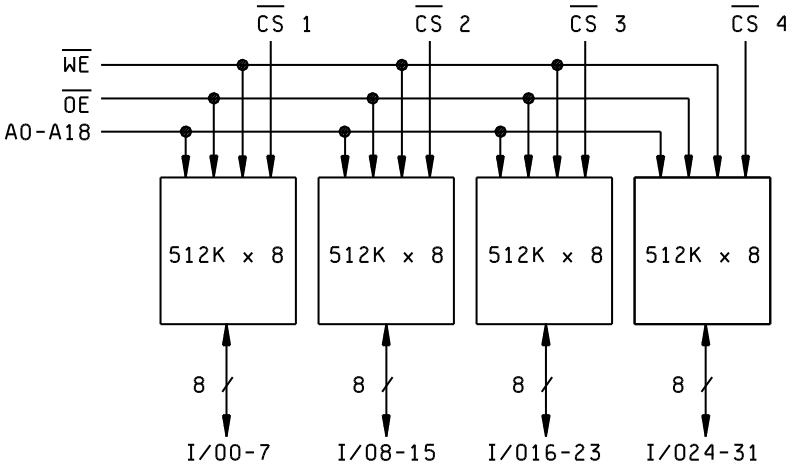
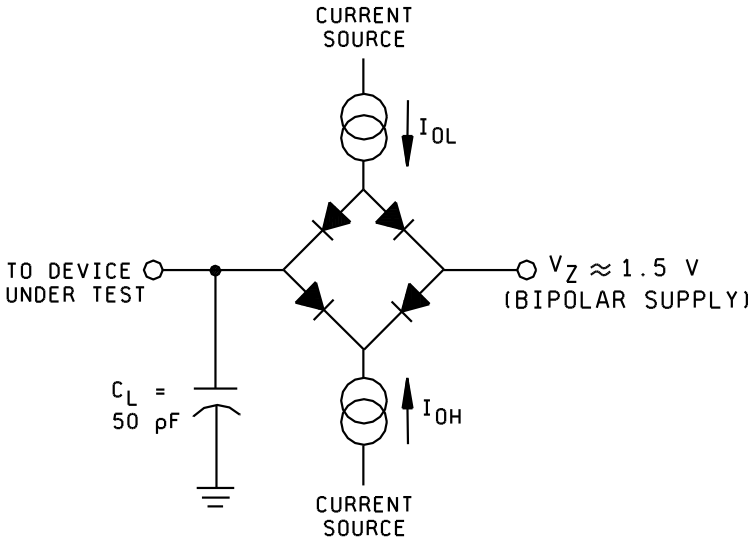


FIGURE 6. Block diagram(s).



Parameter	Typ.	Unit
Input Pulse Level	0 - 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Load Capacitance	50	pf

Notes:
1. V_Z is programmable from +2V to +7V
2. I_{OL} and I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance is Z_0 = 75 ohms.
4. V_Z is typically the midpoint of V_{OL} and V_{OH}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 7. Output load circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical test parameters	1*,2,3,4,7,8A,8B,9,10, 11
Group A test requirements	1,2,3,4,7,8A,8B,9,10, 11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10, 11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups ** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection. Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0526.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000 or telephone (614) 692-0512.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-PRF-38534, MIL-PRF-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-PRF-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-PRF-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply for device classes H and K. Sources of supply for device classes H and K are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-09-27

Approved sources of supply for SMD 5962-94611 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9461101HMC	54230	WS512K32-120G2Q
5962-9461101HMA	54230	WS512K32-120G2Q
5962-9461101HXC	54230	WS512K32N-120H2Q
5962-9461101HXA	54230	WS512K32N-120H2Q
5962-9461101HYC	54230	WS512K32-120G4TQ
5962-9461102HMC	54230	WS512K32-100G2Q
5962-9461102HMA	54230	WS512K32-100G2Q
5962-9461102HXC	54230	WS512K32N-100H2Q
5962-9461102HXA	54230	WS512K32N-100H2Q
5962-9461102HYC	54230	WS512K32-100G4TQ
5962-9461103HMC	54230	WS512K32-85G2Q
5962-9461103HMA	54230	WS512K32-85G2Q
5962-9461103HXC	54230	WS512K32N-85H2Q
5962-9461103HXA	54230	WS512K32N-85H2Q
5962-9461103HYC	54230	WS512K32-85G4TQ
5962-9461104HMC	54230	WS512K32-70G2Q
5962-9461104HMA	54230	WS512K32-70G2Q
5962-9461104HXC	54230	WS512K32N-70H2Q
5962-9461104HXA	54230	WS512K32N-70H2Q
5962-9461104HYC	54230	WS512K32-70G4TQ

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Approved sources of supply for SMD 5962-94611 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9461105HMC	54230	WS512K32-55G2Q
5962-9461105HMA	54230	WS512K32-55G2Q
5962-9461105HMC	88379 2/	ACT-S512K32N-055F2Q
5962-9461105HMA	88379 2/	ACT-S512K32N-055F2Q
5962-9461105HXC	54230	WS512K32N-55H2Q
5962-9461105HXA	54230	WS512K32N-55H2Q
5962-9461105HXC	88379 2/	ACT-S512K32N-055P1Q
5962-9461105HXA	88379 2/	ACT-S512K32N-055P1Q
5962-9461105HYC	88379 2/	ACT-S512K32N-055F1Q
5962-9461105HYA	88379 2/	ACT-S512K32N-055F1Q
5962-9461105HYC	54230	WS512K32-55G4TQ
5962-9461106HMC	54230	WS512K32-45G2Q
5962-9461106HMA	54230	WS512K32-45G2Q
5962-9461106HMC	88379 2/	ACT-S512K32N-045F2Q
5962-9461106HMA	88379 2/	ACT-S512K32N-045F2Q
5962-9461106HXC	54230	WS512K32N-45H2Q
5962-9461106HXA	54230	WS512K32N-45H2Q
5962-9461106HXC	88379 2/	ACT-S512K32N-045P1Q
5962-9461106HXA	88379 2/	ACT-S512K32N-045P1Q
5962-9461106HYC	88379 2/	ACT-S512K32N-045F1Q
5962-9461106HYA	88379 2/	ACT-S512K32N-045F1Q
5962-9461106HYC	54230	WS512K32-45G4TQ
5962-9461107HMC	54230	WS512K32-35G2Q
5962-9461107HMA	54230	WS512K32-35G2Q
5962-9461107HMC	88379	ACT-S512K32N-035F2Q
5962-9461107HMA	88379	ACT-S512K32N-035F2Q
5962-9461107HXC	54230	WS512K32N-35H2Q
5962-9461107HXA	54230	WS512K32N-35H2Q
5962-9461107HXC	88379	ACT-S512K32N-035P1Q
5962-9461107HXA	88379	ACT-S512K32N-035P1Q
5962-9461107HYC	88379	ACT-S512K32N-035F1Q
5962-9461107HYA	88379	ACT-S512K32N-035F1Q
5962-9461107HYC	54230	WS512K32-35G4TQ

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

DATE: 96-09-27

Approved sources of supply for SMD 5962-94611 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9461108HMC	54230	WS512K32-25G2Q
5962-9461108HMA	54230	WS512K32-25G2Q
5962-9461108HMC	88379	ACT-S512K32N-025F2Q
5962-9461108HMA	88379	ACT-S512K32N-025F2Q
5962-9461108HXC	54230	WS512K32N-25H2Q
5962-9461108HXA	54230	WS512K32N-25H2Q
5962-9461108HXC	88379	ACT-S512K32N-025P1Q
5962-9461108HXA	88379	ACT-S512K32N-025P1Q
5962-9461108HYC	88379	ACT-S512K32N-025F1Q
5962-9461108HYA	88379	ACT-S512K32N-025F1Q
5962-9461108HYC	54230	WS512K32-25G4TQ
5962-9461109HMC	54230	WS512K32-20G2Q
5962-9461109HMA	54230	WS512K32-20G2Q
5962-9461109HMC	88379	ACT-S512K32N-020F2Q
5962-9461109HMA	88379	ACT-S512K32N-020F2Q
5962-9461109HXC	54230	WS512K32N-20H2Q
5962-9461109HXA	54230	WS512K32N-20H2Q
5962-9461109HXC	88379	ACT-S512K32N-020P1Q
5962-9461109HXA	88379	ACT-S512K32N-020P1Q
5962-9461109HYC	88379	ACT-S512K32N-020F1Q
5962-9461109HYA	88379	ACT-S512K32N-020F1Q
5962-9461109HYC	54230	WS512K32-20G4TQ
5962-9461110HMC	54230	WS512K32-17G2Q
5962-9461110HMA	54230	WS512K32-17G2Q
5962-9461110HMC	88379 2/	ACT-S512K17N-035F2Q
5962-9461110HMA	88379 2/	ACT-S512K17N-035F2Q
5962-9461110HXC	54230	WS512K32N-17H2Q
5962-9461110HXA	54230	WS512K32N-17H2Q
5962-9461110HXC	88379 2/	ACT-S512K32N-017P1Q
5962-9461110HXA	88379 2/	ACT-S512K32N-017P1Q
5962-9461110HYC	88379 2/	ACT-S512K32N-017F1Q
5962-9461110HYA	88379 2/	ACT-S512K32N-017F1Q
5962-9461110HYC	54230	WS512K32-17G4TQ

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Device types 05, 06, and 10 are not available from the source of supply at this time.

DATE: 96-09-27

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Vendor CAGE number	Vendor name and address
54230	White Microelectronics 4246 East Wood Street Phoenix, AZ 85040-1991
88379	Aeroflex Circuit Technology Corporation 35 South Service Road Plainview, NY 11803